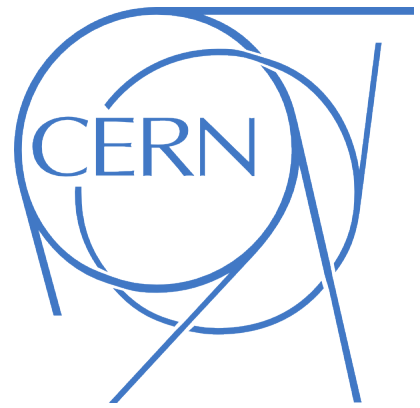




Summer Student Programme (NMS) 2024

A Multipurpose Carrier Board for System-on-Chip (SoC) Modules

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1 Introduction

This project involves the electronics design of a schematic and layout of a carrier board for an FPGA System-on-Chip (SoC) module to be used for the readout of a generic R&D pixel detector such as the ones from the MALTA family. The module selected is the TE0741-05-D2C-1-A [1] from Trenz Electronics. It has an AMD Kintex™ 7 325T-2C and 32 MByte QSPI flash memory. It also has a 3-connector interface that is the similar to many other models. This report outlines the project challenges and the current state of the art.

1.1 Current Status

The MALTA carrier board requires a FPGA evaluation board for data acquisition. Currently, it is connected to commercially available evaluation boards such as the Xilinx 7-series evaluation board, more specifically the KC705 [2] or the Xilinx Virtex VC-707 [3]. The KC705 board is shown in Figure 1.

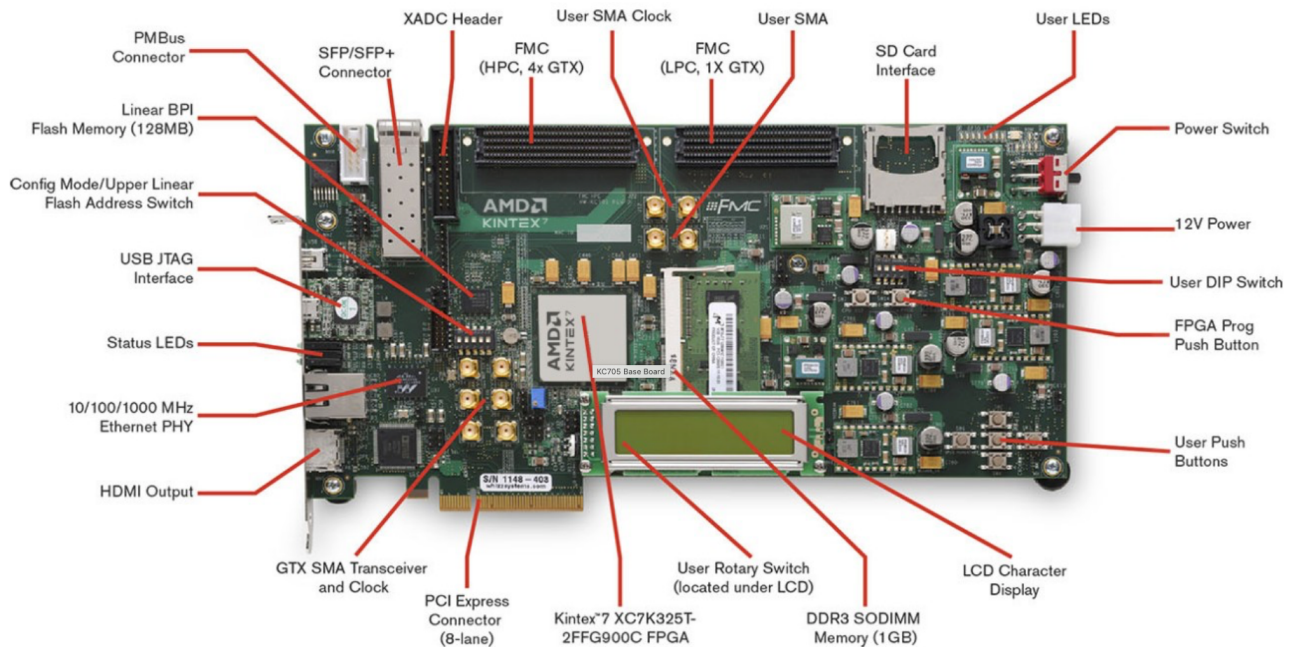


Figure 1: Kintex7 FPGA KC705 Evaluation Kit [2]

The KC705 FPGA kit allows for asynchronous sampling of the data from the FMC Connector using an asynchronous oversampling technique in the FPGA. The hits are then stored in a First-In-First-out (FIFO) and are made available through the ethernet using the IPbus protocol [4].

The current board being used has been discontinued by the manufacturer. It can still be purchased

but some of the components are obsolete. The price is high; directly from AMD, the board retailed for \$2,748. The ethernet controller Marvell Alaska Ethernet 88E1111 present in the KC705, is obsolete and needs to be replaced. An equivalent ethernet controller, which supports the SGMII interface, should be identified and used, as the firmware is only compatible with this particular interface. Alternative boards in consideration will also become obsolete over the years resulting in a similar situation. There are also parts present on the board which is not used in the current set-up. These can be removed and more useful parts such as SMA ports can be added.

2 Proposed Solution and Details of the Multipurpose Carrier Board

Trenz Electronic sells FPGA modules without a carrier board. As previously mentioned, we have considered the TE0741-05-D2C-1-A [1], shown in Figure 2.

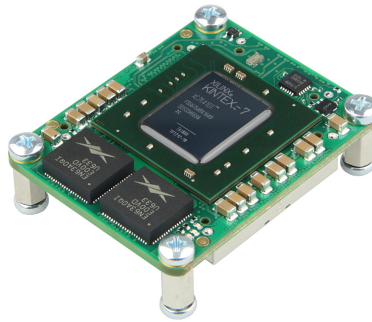


Figure 2: TE0741-05-D2C-1-A FPGA Module [1].

A carrier board is then designed around the module only with required components. The physical footprint, i.e., the dimensions, together with the position of the mounting holes are kept the same. In this way, it fits in the current set-up without any modifications. Only the required components are kept in this design. The list, shown in the table 1, compares the parts in KC705 and the parts that are required and thus present on the Multipurpose Carrier Board. A commercial carrier board cannot be used for this purpose as 2 FMC connectors are required with Gigabit Ethernet. This is currently not available.

This Multipurpose Carrier Board with the TE0741 module significantly brings the cost down. The TE-0741 is currently sold at 854 Euros [1]; the carrier board is estimated to cost 600 CHF. The total cost is hence less than a new FPGA evaluation board from AMD, costing a minimum of ~ 2.6 k USD.

The Multipurpose Carrier Board also avoids the obsolescence problem. With small updates and modifications, the board can fit other FPGA modules. So, even if the selected module is discontinued, it can

Table 1: Components In KC705 Compared to Multipurpose Carrier Board.

Components in KC705	Present in Multipurpose Carrier Board
PM Bus Connector	No
Linear BPI Flash Memory (128 MB)	Yes
Config Mode/Upper Linear Flash Address Switch	Yes
USB JTAG Interface	Yes
Status LEDs	Yes
10/100/1000 MHz Ethernet PHY (RJ46)	Yes
HDMI Output	No
GTX SMA Transceiver and Clock	Yes
PCI Express Connector (8-lane)	No
Kintex-7 XC7K325T	Yes
User Rotary Switch (located under LCD)	No
DDR3 SODIMM Memory (1GB)	No
LCD Character Display	No
User Push Buttons	Yes
FPGA Prog Push Button	Yes
User DIP Switch	Yes
12V Power	Yes
Power Switch	Yes
User LEDs	Yes
SD Card Interface	No
User SMA	Yes
User SMA Clock	Yes
FMC (LCP, 1X GTX)	Yes
FMC (HCP, 4x GTX)	Yes
XADC Header	No
SFP/SFP+ Connector	No

be easily replaced. A large number of modules available fits our requirements. From Trenz Electronic, four more models are available [5].

The Multipurpose Carrier Board allows for 65 Low Voltage Differential Signals (LVDS) at 1 Gbps. This is enough for the current MALTA telescope, which requires less than 50 differential signal pairs. The speed of data transmission is also similar to the KC705 as both FPGAs are the same speed grade of '-2' [6]. Multi-Gigabit Transceiver (MGT) I/O pins are also present; communication over ethernet is therefore possible at 1000 Mb/s. Other non-differential pins are then used for switches and LEDs. The carrier board also has an ethernet controller, and flash memory for data storage.

Since the symbol of TE0741 was not available online or on the CERN Altium library, it was made in Altium Component Maker. It was made available on the CERN Altium library if required for future design modifications of the Multipurpose Carrier Board. The current PCB layout (not completely finished) is

shown in Figure 3.

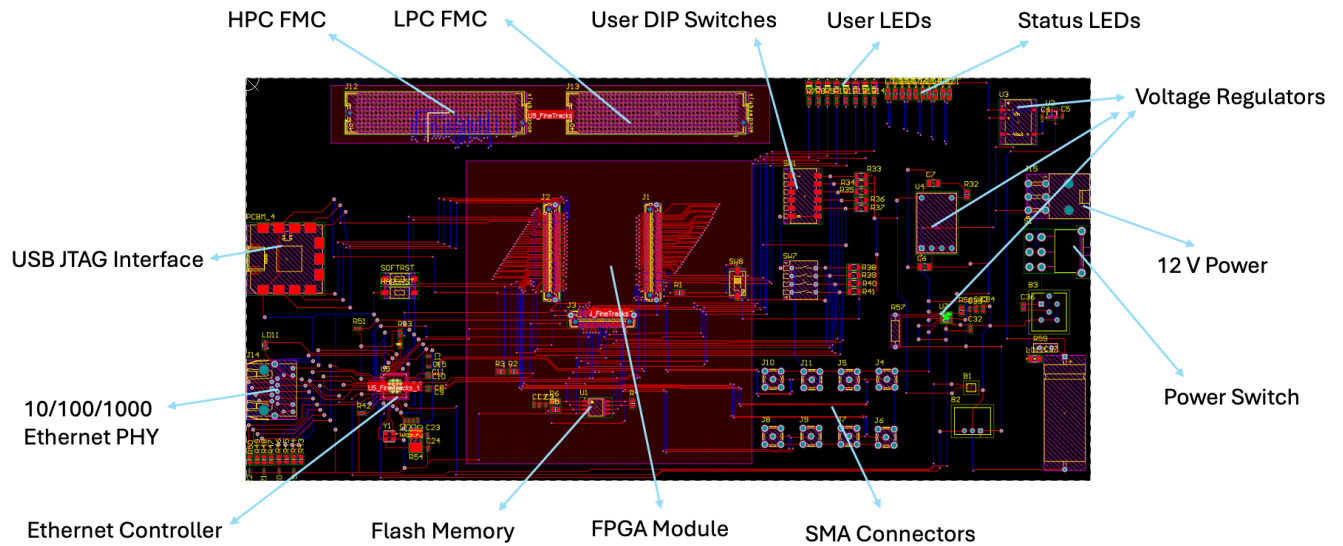


Figure 3: PCB Layout of the Carrier Board.

Comparing to Figure 1, it can be seen that FMC Connectors, USB JTAG Interface, Ethernet PHY, 12 V Power and Power Switch are kept in a similar position. This allows for seamless fitting in the current set-up. The voltage is kept at 12 V with the same power port so that the same power supply can be used. Voltage controllers and regulators are put in place to drop down the voltage to the required 1.0 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V. The components requiring each voltage is shown in table 2.

Table 2: Voltage and Components Requiring the Voltage

Voltage (V)	Component Requiring the Voltage
1.0	Ethernet Controller
1.8	Ethernet Controller
2.5	Ethernet Controller
3.3	Ethernet Controller and TE0741
5.0	TE0741

3 Specification of the Multipurpose Carrier Board

The KC705 FPGA evaluation board uses a high-pin-count (HPC) and a low-pin-count (LPC) FMC connector together with ethernet connection for communication. The same is true for the Multipurpose Carrier Board. The details are discussed below.

3.1 HPC FMC Connector

The HPC FMC connector is used to connect the Multipurpose Carrier Board to the MALTA Carrier Board. The schematic of the FMC connector on Multipurpose Carrier Board is shown in Figure 4 while that on the MALTA Carrier Board in Figure 5. To make it compatible with the current MALTA carrier board, the connections are kept the same. The 'L0 P1' to 'L0 P31' are differential data pins. 'VPULSE' is used to trigger the charge injection circuit. 'RST N LVL' is an active low pin, resetting the FPGA when the voltage is low. 'SC I' and 'SC O' are slow control input and output respectively. 'VREF' serves as a reference voltage to adjust the logic levels. 'TRIGGER I' is clock signal for the periphery. The frequency goes as high as 40 MHz.

'SC LOAD' present in the Multipurpose Carrier Board, is a slow control lead. The configuration of the chip is sent through 'SC I' pins to the chip. Enabling 'SC LOAD' for one clock cycle causes the chip to load the configuration in memory. This was implemented in MALTA 2. Therefore, it is absent from the schematic in Figure 5 as the latter is from MALTA 1.

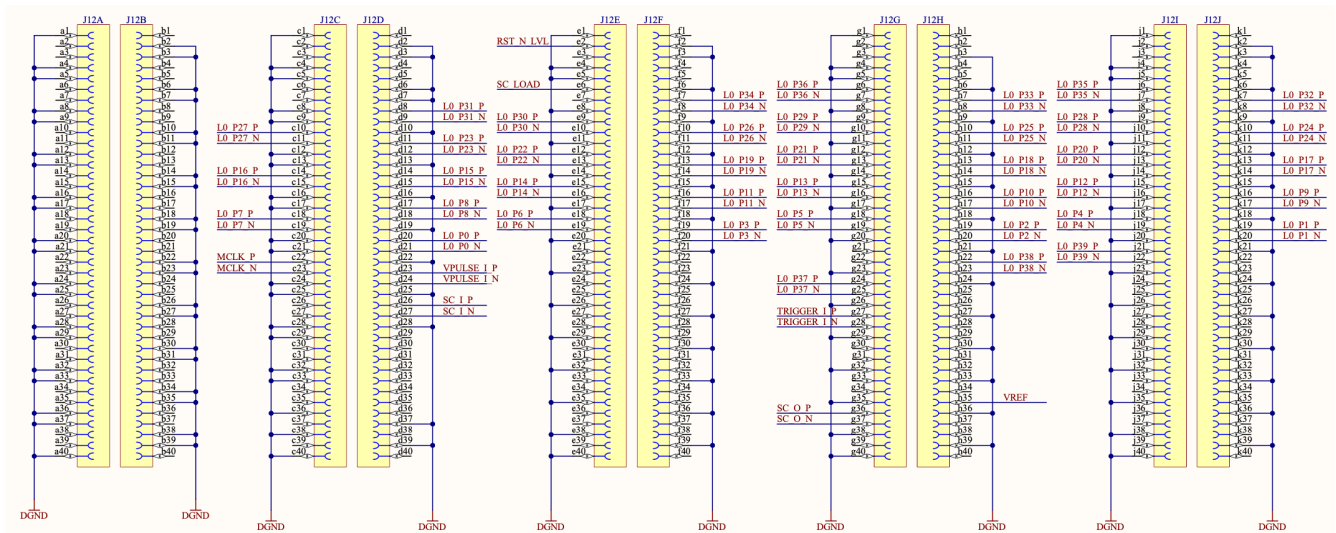


Figure 4: HPC FMC on the Multipurpose Carrier Board

3.2 LPC FMC Connector

LPC FMC connector, shown in Figure 6 is mainly used to increase the number of SMA connectors. LEDs are also present to visualise data transmission. Resistors present prevent damage to the LEDs when the voltage is higher then the voltage threshold of the latter.

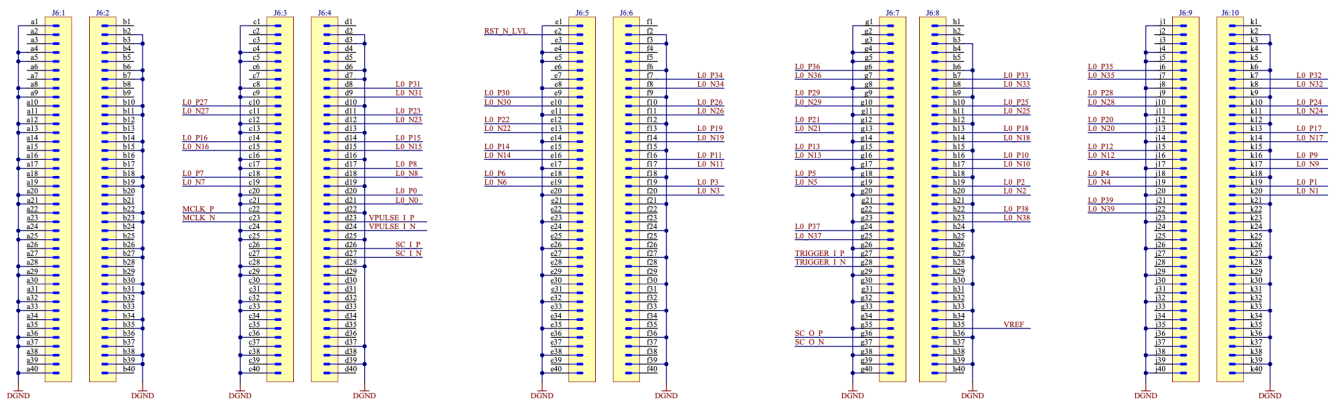


Figure 5: HPC FMC on the MALTA Carrier Board

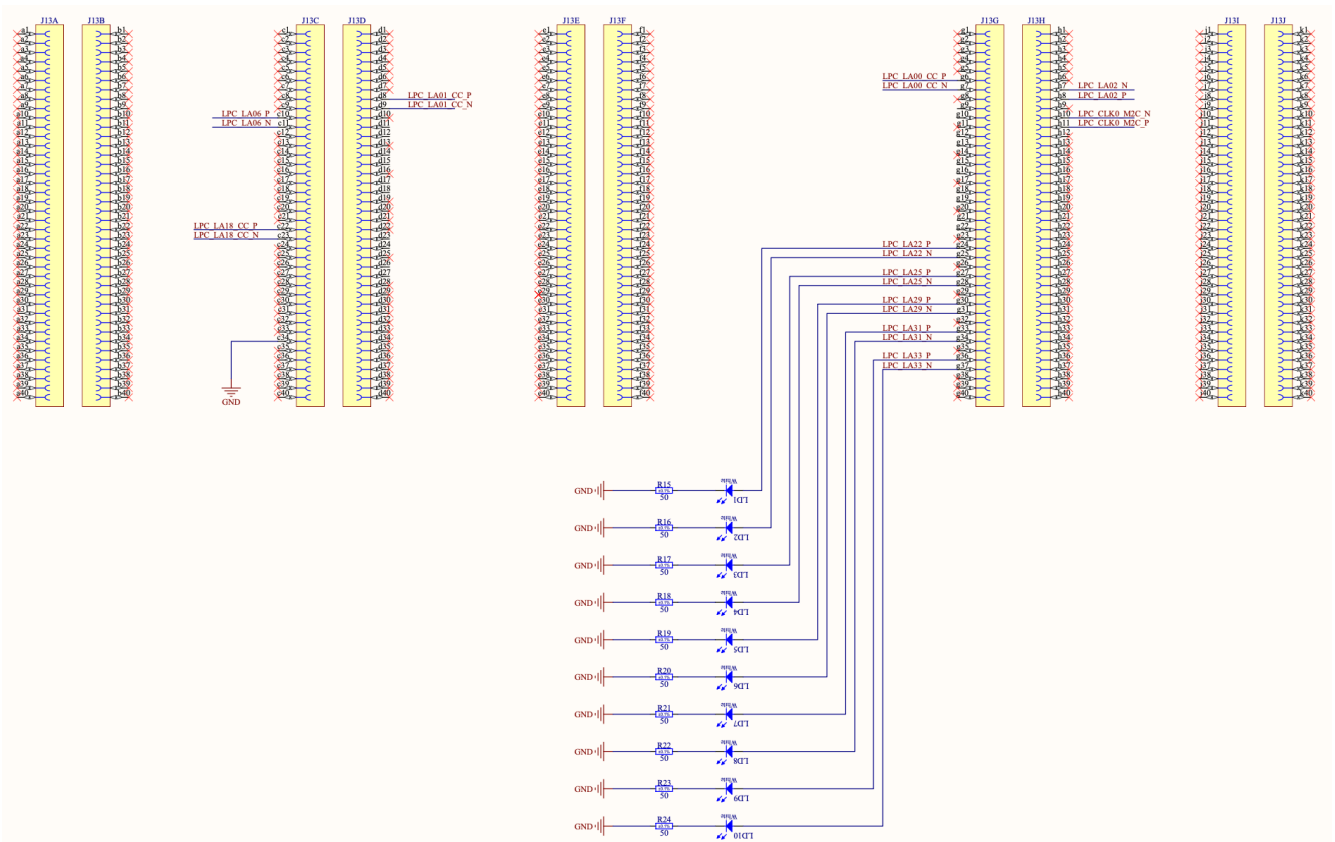


Figure 6: LPC FMC on the MALTA Carrier Board

3.3 Ethernet Controller

The current FPGA Evaluation Kit KC705 uses a Marvell Alaska 88E1111 as ethernet controller. As previously mentioned, the latter is obsolete and has been termed as a legacy product by the manufacturer [7]. Therefore, for the Multipurpose Carrier Board, the DP83867ERGZR ethernet controller from Texas Instrument is used [8]. It allows for data transfer at 1000 Mb/s with the required SGMII interface. Its pin configuration is shown in Figure 7. The pin functions are described in the Figure 8.

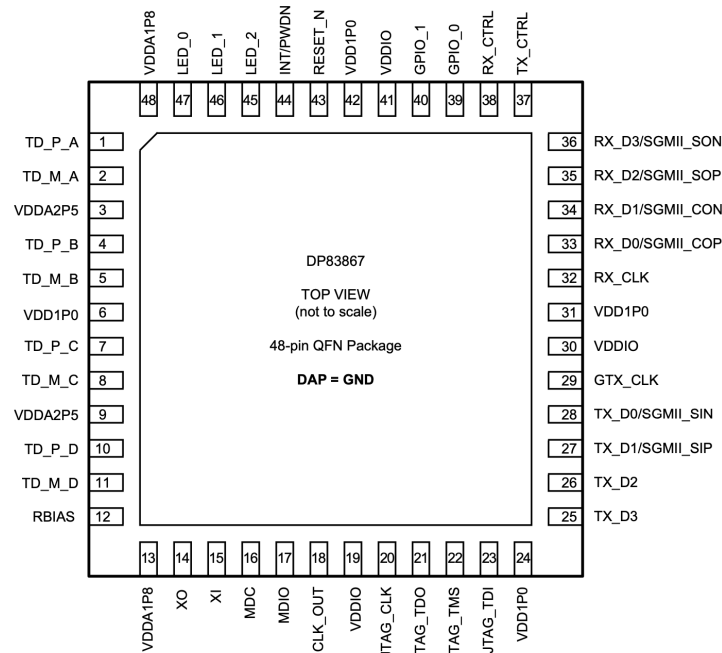


Figure 7: Pin Configuration of the Ethernet Controller.

The SGMII interface is planned to be used as it is the only interface supported by the IPbus protocol. Therefore, pins corresponding only to this interface is routed while those for the RGMII interface are not connected. Other pins such as for power (1.0 V, 1.8 V, 2.5 V, 3.3 V) and resets are also linked. The differential signal pair is routed to the FPGA module through MGT pins to allow for data transfer at 1000 Mb/s. The MDC and MDIO pins are also linked to the FPGA module. Three differential pairs are connected between the ethernet controller and the PHY. Capacitors and resistors are routed accordingly to cancel DC voltages and reduce noise level through RC filtering. LEDs are used to indicate when a link is established (LED LINK ACT), when there is traffic (LED TRAFFIC) and when the connection is at 1000 MB/s (LED LINK 1000). The completed schematic is shown in Figure 9. The PHY is shown in Figure 10.

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
MAC INTERFACES (SGMII, RGMII)			
TX_D3	25	I, PD	TRANSMIT DATA Bit 3: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
TX_D2	26	I, PD	TRANSMIT DATA Bit 2: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
SGMII_SIP	27	I, PD	Differential SGMII Data Input: This signal carries data from the MAC to the PHY in SGMII mode. It is synchronous to the differential SGMII clock input. This pin should be AC-coupled to the MAC through a 0.1μF capacitor when operating in SGMII mode.
TX_D1	27	I, PD	TRANSMIT DATA Bit 1: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
SGMII_SIN	28	I, PD	Differential SGMII Data Input: This signal carries data from the MAC to the PHY in SGMII mode. It is synchronous to the differential SGMII clock input. This pin should be AC-coupled to the MAC through a 0.1μF capacitor when operating in SGMII mode.
TX_D0	28	I, PD	TRANSMIT DATA Bit 0: This signal carries data from the MAC to the PHY in RGMII mode. It is synchronous to the transmit clock GTX_CLK.
GTX_CLK	29	I, PD	RGMII TRANSMIT CLOCK: This continuous clock signal is sourced from the MAC layer to the PHY. Nominal frequency is 125MHz.
RX_CLK	32	O	RGMII RECEIVE CLOCK: Provides the recovered receive clocks for different modes of operation: 2.5MHz in 10Mbps mode. 25MHz in 100Mbps mode. 125MHz in 1000Mbps mode.
SGMII_COP	33	S, O	Differential SGMII Clock Output: This signal is a continuous 625MHz clock signal driven by the PHY in SGMII mode. This pin should be AC-coupled to the MAC through a 0.1μF capacitor when operating in SGMII mode.
RX_D0	33	S, O, PD	RECEIVE DATA Bit 0: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.
SGMII_CON	34	S, O, PD	Differential SGMII Clock Output: This signal is a continuous 625MHz clock signal driven by the MAC in SGMII mode. This pin should be AC-coupled to the MAC through a 0.1μF capacitor when operating in SGMII mode.
RX_D1	34	O, PD	RECEIVE DATA Bit 1: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.
SGMII_SOP	35	S, O, PD	Differential SGMII Data Output: This signal carries data from the PHY to the MAC in SGMII mode. It is synchronous to the differential SGMII clock output. This pin should be AC-coupled to the MAC through a 0.1μF capacitor when operating in SGMII mode.
RX_D2	35	S, O, PD	RECEIVE DATA Bit 2: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.
SGMII_SON	36	S, O, PD	Differential SGMII Data Output: This signal carries data from the PHY to the MAC in SGMII mode. It is synchronous to the differential SGMII clock output. This pin should be AC-coupled to the MAC through a 0.1μF capacitor when operating in SGMII mode.
RX_D3	36	O, PD	RECEIVE DATA Bit 3: This signal carries data from the PHY to the MAC in RGMII mode. It is synchronous to the receive clock RX_CLK.
TX_CTRL	37	I, PD	TRANSMIT CONTROL: In RGMII mode, it combines the transmit enable and the transmit error signals of GMII mode using both clock edges.
RX_CTRL	38	S, O, PD	RECEIVE CONTROL: In RGMII mode, the receive data available and receive error are combined (RXDV_ER) using both rising and falling edges of the receive clock (RX_CLK).
GENERAL-PURPOSE I/O			

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
GPIO_0	39	S, O, PD	General-Purpose I/O: This signal provides a multi-function configurable I/O. Refer to the GPIO_MUX_CTRL register for details.
GPIO_1	40	S, O, PD	General-Purpose I/O: This signal provides a multi-function configurable I/O. Refer to the GPIO_MUX_CTRL register for details.
MANAGEMENT INTERFACE			
MDC	16	I, PD	MANAGEMENT DATA CLOCK: Synchronous clock to the MDIO serial management input and output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25MHz and no minimum.
MDIO	17	I/O	MANAGEMENT DATA I/O: Bidirectional management instruction and data signal that may be sourced by the management station or the PHY. This pin requires pullup resistor. The IEEE specified resistor value is 1.5kΩ, but a 2.2kΩ is acceptable.
INT / PWDN	44	I/O, PU	INTERRUPT / POWER DOWN: The default function of this pin is POWER DOWN. POWER DOWN: This is an Active Low Input. Asserting this signal low enables the power-down mode of operation. In this mode, the device powers down and consume minimum power. Register access is available through the Management Interface to configure and power up the device. INTERRUPT: When operating this pin as an interrupt, it is an open-drain architecture. TI recommends using an external 2.2kΩ resistor connected to the VDDIO supply.
RESET			
RESET_N	43	I, PU	RESET: The active low RESET initializes or reinitializes the DP83867. All internal registers re-initialize to their default state upon assertion of RESET. The RESET input must be held low for a minimum of 1μs.
CLOCK INTERFACE			
XI	15	I	CRYSTAL/OSCILLATOR INPUT: 25MHz oscillator or crystal input (50 ppm)
XO	14	O	CRYSTAL OUTPUT: Second terminal for 25MHz crystal. Must be left floating if a clock oscillator is used.
CLK_OUT	18	O	CLOCK OUTPUT: Output clock
JTAG INTERFACE			
JTAG_CLK	20	I, PU	JTAG TEST CLOCK: IEEE 1149.1 Test Clock input, primary clock source for all test logic input and output controlled by the testing entity.
JTAG_TDO	21	O	JTAG TEST DATA OUTPUT: IEEE 1149.1 Test Data Output pin, the most recent test results are scanned out of the device through TDO.
JTAG_TMS	22	I, PU	JTAG TEST MODE SELECT: IEEE 1149.1 Test Mode Select pin, the TMS pin sequences the Tap Controller (16-state FSM) to select the desired test instruction. TI recommends applying 3 clock cycles with JTAG_TMS high to reset the JTAG.
JTAG_TDI	23	I, PU	JTAG TEST DATA INPUT: IEEE 1149.1 Test Data Input pin, test data is scanned into the device through TDI.
LED INTERFACE			
LED_2	45	S, I/O, PD	LED_2: By default, this pin indicates receive or transmit activity. Additional functionality is configurable through LEDCR1[11:8] register bits.
LED_1	46	S, I/O, PD	LED_1: By default, this pin indicates that 1000BASE-T link is established. Additional functionality is configurable through LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	LED_0: By default, this pin indicates that link is established. Additional functionality is configurable through LEDCR1[3:0] register bits.
MEDIA DEPENDENT INTERFACE			
TD_P_A	1	A	Differential Transmit and Receive Signals
TD_M_A	2	A	Differential Transmit and Receive Signals
TD_P_B	4	A	Differential Transmit and Receive Signals
TD_M_B	5	A	Differential Transmit and Receive Signals

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
TD_P_C	7	A	Differential Transmit and Receive Signals
TD_M_C	8	A	Differential Transmit and Receive Signals
TD_P_D	10	A	Differential Transmit and Receive Signals
TD_M_D	11	A	Differential Transmit and Receive Signals
OTHER PINS			
RBIAS	12	A	Bias Resistor Connection. A 11k Ω $\pm$ 1% resistor should be connected from RBIAS to GND.
POWER AND GROUND PINS			
VDDA2P5	3, 9	P	2.5V Analog Supply ($\pm$ 5%). Each pin requires a 1 μ F and 0.1 μ F capacitor to GND.
VDD1P0	6, 24, 31, 42	P	1V Analog Supply (+15.5%, -5%). Each pin requires a 1 μ F and 0.1 μ F capacitor to GND.
VDDA1P8	13, 48	P	1.8V Analog Supply ($\pm$ 5%). No external supply is required for this pin. When unused, no connections should be made to this pin. For additional power savings, an external 1.8V supply can be connected to these pins. When using an external supply, each pin requires a 1 μ F and 0.1 μ F capacitor to GND.
VDDIO	19, 30, 41	P	I/O Power: 1.8V ($\pm$ 5%), 2.5V ($\pm$ 5%) or 3.3V ($\pm$ 5%). Each pin requires a 1 μ F and 0.1 μ F capacitor to GND
GND	Die Attach Pad	P	Ground

Figure 8: Pin Configuration of Ethernet Controller [8]

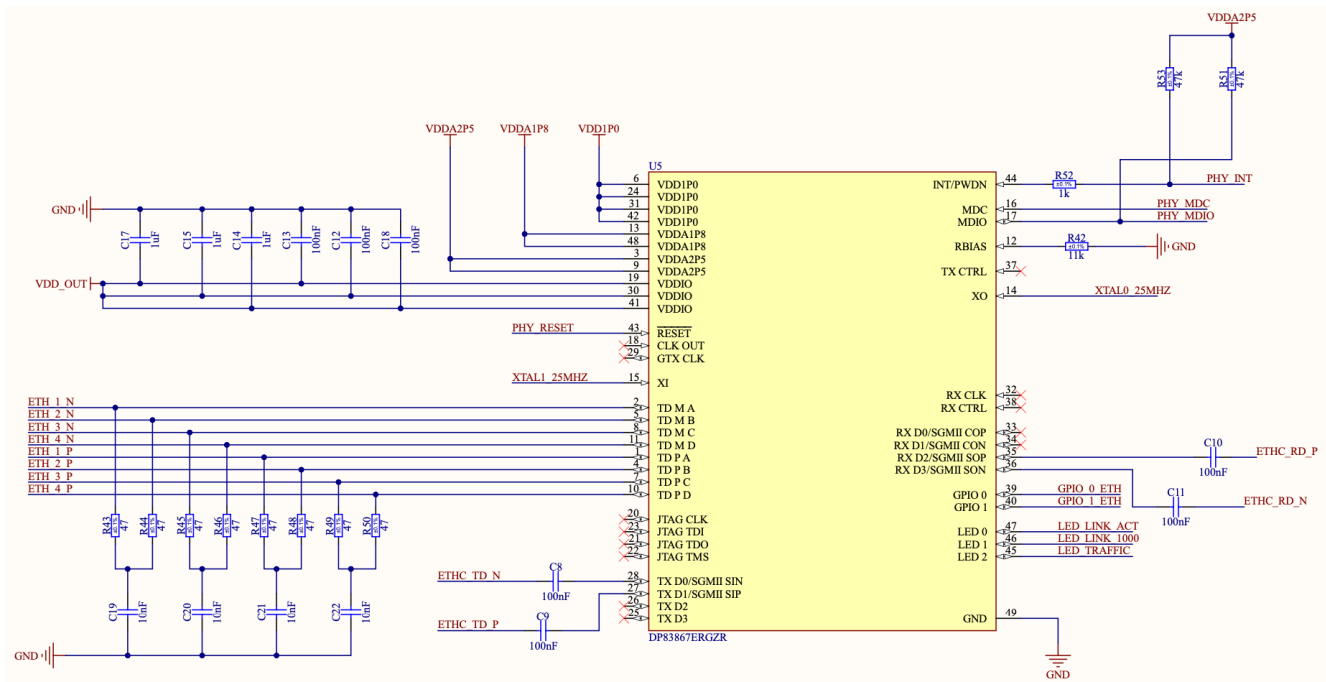


Figure 9: Schematic of Ethernet Controller

An oscillator is also present to produce a periodic electronic signal at 25.00 MHz. This signal is required for the proper transmission and reception of data packets. The schematic of the oscillator is shown in Figure 11.

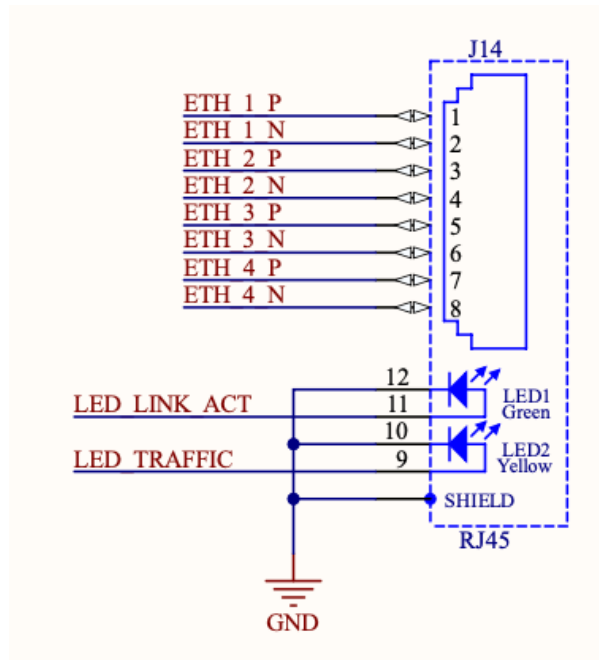


Figure 10: Schematic of Ethernet PHY

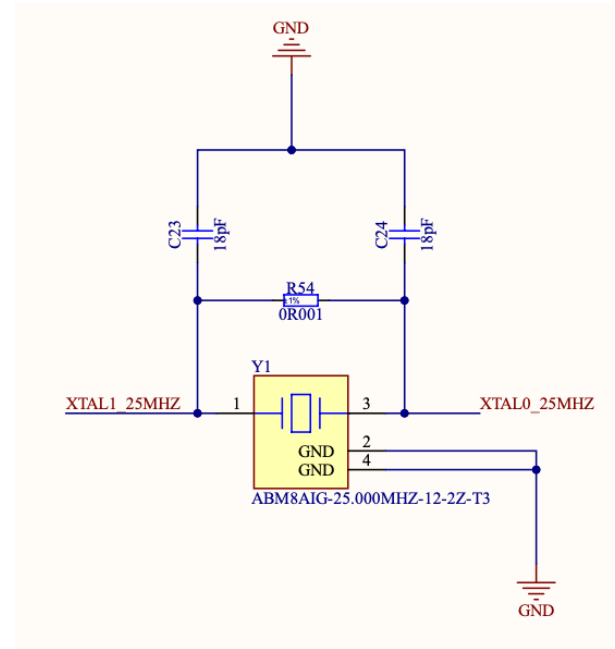


Figure 11: Schematic of Oscillator

4 Conclusion and Future Work

The schematic of the Multipurpose Carrier Board has been completed. Layout has also been started with about 75% completed. The estimated time required to finish the routing is about 2 weeks. After that, the PCB will be sent for a quotation, followed by manufacturing and assembly. Testing and verification will then be carried out.

Currently, the MALTA Telescope uses 6 FPGA boards; one board is used on each plane. This is a limitation of the FPGA; the latter does not have enough LVDS I/O pins to support two MALTA Carrier Boards. The TE0741 has 65 LVDS and each MALTA Carrier Board requires 45. Therefore, each FPGA can only support a single MALTA Carrier Board. Future improvement could involve the use of an FPGA which has at least 90 LVDS pins. Thus, one Multipurpose Carrier Board will be able to connect to two MALTA Carrier Boards. The number of FPGA required is cut in half and cost is also reduced.

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